WHAT IS CLAIMED IS:

1. A semiconductor integrated circuit device having logic gates constructed of switching elements formed on a semiconductor substrate, which performs given processing by the logic gates on at least one input signal and outputs at least one signal, the switching elements being composed of at least two kinds of switching elements, a first kind each with a low threshold voltage and a second kind each with a high threshold voltage, wherein there are provided a plurality of paths from which the signals are transmitted, in which each of switching elements constituting a logic gate on a first path has a different threshold voltage from that of each of switching elements constituting a logic gate on a second path.

2. A semiconductor integrated circuit device having logic gates constructed of switching elements formed on a semiconductor substrate, which performs given processing by the logic gates on at least one input signal and outputs at least one signal, the switching elements being composed of at least two kinds of switching elements, a first kind each with a low threshold voltage and a second kind each with a high threshold voltage, wherein there are provided a mixture of a logic gate constructed of switching elements each with a low threshold voltage and a logic gate constructed of

switching elements each with a high threshold voltage on one path from which a signal is transmitted.

3. A semiconductor integrated circuit device having logic gates constructed of switching elements formed on a semiconductor substrate, which performs given processing by the logic gates on at least one input signal and outputs at least one signal, the switching elements being composed of at least two kinds of switching elements, a first kind each with a low threshold voltage and a second kind each with a high threshold voltage, wherein there are provided signal paths composed of a signal path from a first node to a second node, a signal path from the second node to a third node and a signal path from the second node to a fourth node, wherein a ratio of the number of logic gates constructed of switching elements each with a low threshold value to the total number of logic gates on the path from the first node to the second node, is larger than a ratio of the number of logic gates constructed of switching elements each with a low threshold value to the total number of logic gates on the path from the second node to the third node, or the path from the second node to the fourth node.

4. A semiconductor integrated circuit device having logic gates constructed of switching elements formed on a semiconductor substrate, which performs given processing by the logic gates on at least one input signal and outputs at

least one signal, the switching elements being composed of at least two kinds of switching elements, a first kind each with a low threshold voltage and a second kind each with a high threshold voltage, wherein there are provided signal paths composed of a signal path from a first node to a second node, a signal path from the third node to a second node and a signal path from the second node to a fourth node, wherein a ratio of the number of logic gates constructed of switching elements each with a low threshold value to the total number of logic gates on the path from the second node to the fourth node, is larger than a ratio of the number of logic gates constructed of switching elements each with a low threshold value to the total number of logic gates on each of the paths from the first node to the second node and from the third node to the second node.

5. A semiconductor integrated circuit device according to any of claims 1 to 4, wherein the paths from which the signals are transmitted are three kinds of paths: a first path is a path from an input pin of the semiconductor integrated circuit to an input pin of a state holding circuit which the signal reaches for the first time; a second path is a path from an output pin of the state holding circuit to an input pin of a second state holding circuit which the signal reaches for the second time; and a third path is a path from the second state holding circuit to an output pin

of the semiconductor integrated circuit without transmitting a third state holding circuit, or part of each of the three kinds of paths.

6. A semiconductor integrated circuit device having logic gates constructed of switching elements formed on a semiconductor substrate, which performs given processing by the logic gates on at least one input signal and outputs at least one signal,

comprising:

at least first and second state holding circuits;

at least first, second, third and fourth switching elements;

a first operating potential supply line by which a first operating potential point is supplied with electricity and a second operating potential supply line by which a second operating potential point is supplied with electricity; and first and second nodes,

wherein an output pin of the first state holding circuit or an input pin of the semiconductor integrated circuit is connected to gates electrodes of the first and second switching elements directly or through at least one logic gate;

the first switching element is connected to the first operating potential point and the first node so that a source/drain path lies therebetween;

the second switching element is connected to the second operating potential point and the first node so that a source/drain path lies therebetween;
the first node is connected to gate electrodes of the third and fourth switching elements;
the third switching element is connected to the first operating potential point and the second node so that a source/drain path lies therebetween;
the fourth switching element is connected to the second operating potential point and the second node so that a source/drain path lies therebetween; and
the second node is connected to an input pin of the second state holding circuit or an output pin of the semiconductor integrated circuit directly or through at least one logic gate,
wherein a threshold voltage of the first switching element is different from a threshold voltage of the third switching element, or a threshold voltage of the second switching element is different from a threshold of the fourth switching element.

7. A semiconductor integrated circuit device having logic gates constructed of switching elements formed on a semiconductor substrate, which performs given processing by the logic gates on at least one input signal and outputs at least one signal,

comprising:
at least first, second and third state holding circuits;
at least first, second, third, fourth, fifth and sixth switching elements;
a first operating potential supply line by which a first operating potential point is supplied with electricity and a second operating potential supply line by which a second operating potential point is supplied with electricity; and first, second and third nodes,
wherein an output pin of the first state holding circuit or an input pin of the semiconductor integrated circuit is connected to gates electrodes of the first and second switching elements directly or through at least one logic gate;
the first switching element is connected to the first operating potential point and the first node so that a source/drain path lies therebetween;
the second switching element is connected to the second operating potential point and the first node so that a source/drain path lies therebetween;
the first node is connected to gate electrodes of the third, fourth, fifth and sixth switching elements;
the third switching element is connected to the first operating potential point and the second node so that a source/drain path lies therebetween;

the fourth switching element is connected to the second operating potential point and the second node so that a source/drain path lies therebetween;
the fifth switching element is connected to the first operating potential point and the third node so that a source/drain path lies therebetween;
the sixth switching element is connected to the second operating potential point and the third node so that a source/drain path lies therebetween;
the second node is connected to an input pin of the second state holding circuit or an output pin of the semiconductor integrated circuit directly or through at least one logic gate; and
the third node is connected to an input pin of the third state holding circuit or an output pin of the semiconductor integrated circuit directly or through at least one logic gate,
wherein a threshold voltage of the third switching element is higher than a threshold voltage of the first switching element, or a threshold voltage of the fourth switching element is higher than a threshold of the second switching element.

8. A semiconductor integrated circuit device having logic gates constructed of switching elements formed on a semiconductor substrate, which performs given processing by

the logic gates on at least one input signal and outputs at least one signal,

comprising:

at least first, second and third state holding circuits;

at least first, second, third, fourth, fifth, sixth, seventh and eighth switching elements;

a first operating potential supply line by which a first operating potential point is supplied with electricity and a second operating potential supply line by which a second operating potential point is supplied with electricity; and first, second and third nodes,

wherein an output pin of the first state holding circuit or an input pin of the semiconductor integrated circuit is connected to gate electrodes of the first and second switching elements directly or through at least one logic gate;

the first switching element is connected to the first operating potential point and the first node so that a source/drain path lies therebetween;

the second switching element is connected to the second operating potential point and the first node so that a source/drain path lies therebetween;

an output pin of the second state holding circuit or an input pin of the semiconductor integrated circuit is connected to

gate electrodes of the third and fourth switching elements directly or through at least one logic gate;
the third switching element is connected to the first operating potential point and the second node so that a source/drain path lies therebetween;
the fourth switching element is connected to the second operating potential point and the second node so that a source/drain path lies therebetween;
the first node is connected to gate electrodes of the fifth and sixth switching elements;
the second node is connected to gate electrodes of the seventh and eighth switching elements;
the fifth and seventh switching elements are connected to the first operating potential point and the third node so that source/drain paths lie therebetween;
the sixth and eighth switching elements are connected to the second operating potential point and the third node so that source/drain paths lie therebetween; and
the third node is connected to an input pin of the third state holding circuit or an output pin of the semiconductor integrated circuit directly or through at least one logic gate,
wherein a threshold voltage of the first switching element is higher than a threshold voltage of the fifth or seventh switching element, or a threshold voltage of the second

switching element is higher than a threshold voltage of the sixth or eighth switching element.

9. A semiconductor integrated circuit device having logic gates constructed of switching elements formed on a semiconductor substrate, which performs given processing by the logic gates on at least one input signal and outputs at least one signal,
comprising:
at least first, second and third state holding circuits;
at least first, second, third, fourth, fifth and sixth switching elements;
a first operating potential supply line by which a first operating potential point is supplied with electricity and a second operating potential supply line by which a second operating potential point is supplied with electricity;
first, second and third nodes; and
first and second logic gate groups in each of which a plurality of logic gates are in series connected;
wherein an output pin of the first state holding circuit or an input pin of the semiconductor integrated circuit is connected to gate electrodes of the first and second switching elements directly or through at least one logic gate;

the first switching element is connected to the first operating potential point and the first node so that a source/drain path lies therebetween;
the second switching element is connected to the second operating potential point and the first node so that a source/drain path lies therebetween;
the first node is connected to gate electrodes of the third, fourth, fifth and sixth switching elements;
the third switching element is connected to the first operating potential point and the second node so that a source/drain path lies therebetween;
the fourth switching element is connected to the second operating potential point and the second node so that a source/drain path lies therebetween;
the fifth switching elements is connected to the first operating potential point and the third node so that source/drain paths lie therebetween;
the sixth switching element is connected to the second operating potential point and the third node so that source/drain paths lie therebetween;
the second node is connected to an input pin of the second state holing circuit through the first logic gate group; and
the third node is connected to an input pin of the third state holing circuit through the second logic gate group,

wherein the first logic gate group is larger in number of logic gate stages than the second logic gate group, and wherein a threshold voltage of the fifth switching element is higher than a threshold voltage of each of the first and third switching elements, or a threshold voltage of the sixth switching element is higher than a threshold voltage of each of the second and fourth switching elements.

10. A semiconductor integrated circuit device having logic gates constructed of switching elements formed on a semiconductor substrate, which performs given processing by the logic gates on at least one input signal and outputs at least one signal,

comprising:

at least first, second and third state holding circuits;

at least first, second, third, fourth, fifth, sixth, seventh and eighth switching elements;

a first operating potential supply line by which a first operating potential point is supplied with electricity and a second operating potential supply line by which a second operating potential point is supplied with electricity;

first, second and third nodes; and

first and second logic gate groups in each of which a plurality of logic gates are in series connected;

wherein an output pin of the first state holding circuit is connected to gate electrodes of the first and second switching elements through the first logic gate group;
the first switching element is connected to the first operating potential point and the first node so that a source/drain path lies therebetween;
the second switching element is connected to the second operating potential point and the first node so that a source/drain path lies therebetween;
an output pin of the second state holding circuit is connected to gate electrodes of the third and fourth switching elements through the first logic group;
the third switching element is connected to the first operating potential point and the second node so that a source/drain path lies therebetween;
the fourth switching element is connected to the second operating potential point and the second node so that a source/drain path lies therebetween;
the first node is connected to gate electrodes of the fifth and sixth switching elements;
the second node is connected to gate electrodes of the seventh and eighth switching elements;
the fifth and seventh switching elements are connected to the first operating potential point and the third node so that source/drain paths lie therebetween;

the sixth and eighth switching elements are connected to the second operating potential point and the third node so that source/drain paths lie therebetween; and

the third node is connected to an input pin of the third state holing circuit or an output pin of the semiconductor integrated circuit directly or through at least one logic gate,

wherein the first logic gate group is larger in number of logic gate stages than the second logic gate group, and

wherein a threshold voltage of the third switching element is higher than a threshold voltage of each of the first and fifth switching elements or a threshold voltage of the seventh switching element, or a threshold voltage of the fourth switching element is higher than a threshold voltage of each of the second and sixth switching elements or a threshold voltage of the eighth switching element.

11. A semiconductor integrated circuit device having logic gates constructed of switching elements formed on a semiconductor substrate, which performs given processing by the logic gates on at least one input signal and outputs at least one signal,

comprising:

at least first, second and third switching elements;

a first operating potential supply line by which a first operating potential point is supplied with electricity and

a second operating potential supply line by which a second operating potential point is supplied with electricity; and first, second and third nodes,
wherein the first node is connected to a gate electrode of the first switching element;
the second node is connected to a drain electrode of the first switching element;
a source electrode of the first switching element is connected to gate electrodes of the second and third switching elements;
the second switching element is connected to the first operating potential point and the third node so that a source/drain path lies therebetween; and
the third switching element is connected to the second operating potential point and the third node so that a source/drain path lies therebetween,
wherein a signal is input to the first and second nodes and a signal is output from the third node and
wherein a threshold voltage of the first switching element is lower than a threshold voltage of each of the second and third switching elements.

12. A semiconductor integrated circuit device according to any of claims 1 to 11, wherein the means for providing switching elements with different threshold

voltages is to change an impurity density of a semiconductor substrate under a gate oxide film of a switching element.

13. A semiconductor integrated circuit device according to any of claims 1 to 11, wherein the means for providing switching elements with different threshold voltages is to change a bias voltage value supplied to a substrate of a switching element.

14. A semiconductor integrated circuit device according to any of claims 1 to 11, wherein the means for providing switching elements with different threshold voltages is to change a thickness of a gate oxide film of a switching element.

15. A semiconductor integrated circuit device according to any of claims 1 to 11, wherein the means for providing switching elements with different threshold voltages is to change a gate length of a switching element.

16. A semiconductor integrated circuit device according to any of claims 1 to 11, wherein the means for providing switching elements with different threshold voltages is to combine two or more selected from the group consisting of first means to change an impurity density of a semiconductor substrate under a gate oxide film of a switching element; second means to change a bias voltage value supplied to a substrate of a switching element; third means to change a thickness of a gate oxide film of a

switching element; and fourth means to change a gate length of a switching element.

17. A semiconductor integrated circuit device according to claim 13, wherein logic gates are arranged one dimensionally in one line and a plurality of rows of logic gates are arranged in directions perpendicular to the one line so as to dispose logic gates two dimensionally, comprising substrate bias operating potential supply lines provided in parallel to the rows and in number equal to the number of kinds of threshold voltages of the switching elements in use.

18. A semiconductor integrated circuit device according to claim 13, comprising a plurality of well regions which are mutually insulated, wherein the switching elements with different threshold voltages are formed on different well regions.

19. A semiconductor integrated circuit device according to claim 18, wherein logic gates are arranged one dimensionally in one line and a plurality of rows of logic gates are arranged in directions perpendicular to the one line so as to dispose logic gates two dimensionally, and wherein logic gates which are constructed of switching elements with the same threshold voltage are arranged on one row; and the one row is disposed on one well region aligned along the one row; and there is provided with an operating

potential supply line in parallel to a row in order to supply a substrate bias source.

20. A semiconductor integrated circuit device according to claim 19, wherein when logic gates on a plurality of rows adjacent one another are constructed of switching elements each with the same threshold voltage, the plurality of rows own commonly one well region among them.

21. A storage medium on which there is stored a cell library, a logic circuit component having a specific logic function designed in advance, in which there are written a function, shape, delay, consumption power and the like of each cell,

wherein the cell library is registered with at least two kinds of cells which are different in a delay and consumption power because of being constructed of switching elements which have different threshold voltages while having the same function and the same shape.

22. A designing method for a semiconductor integrated circuit device according to any of claims 1 to 20, using the storage medium on which there is stored the cell library according to claim 21, comprising at least the steps of:

calculating consumption power and a delay of a signal path; and

assigning to a logic circuit one cell selected among at least two kinds of cells constructed of switching elements which

have different threshold voltages while having the same function and the same shape, using the result of the step of calculating consumption power and a delay of a signal path.

23. A designing method for a semiconductor integrated circuit according to any of claims 1 to 20, using the storage medium on which there is stored the cell library according to claim 21, comprising at least the steps of:

designing a logic circuit using only cells constructed of switching elements each with a high threshold value;

calculating consumption power and a delay of a signal path; and

replacing a part of the logic circuit designed using only cells constructed of switching elements each with a high threshold value, by a cell constructed of switching elements each of which has a low threshold value while having the same function and the same size.

24. A semiconductor integrated circuit comprising a plurality of circuits each of which includes at least one selected from the group consisting of a latch circuit, a flip-flop circuit, a signal output terminal and a signal input terminal in a signal path, wherein there are provided a plurality of transistors with different threshold values in paths between the circuits.

25. A semiconductor integrated circuit comprising a plurality of first circuits controlled by a clock signal in a signal path and a second circuit including a plurality of transistors with different threshold values inserted between the first circuits.

26. A designing method for a semiconductor integrated circuit in which a plurality of first circuits controlled by a clock signal are included in a signal path and a second circuit constructed of a plurality of transistors with different threshold values is inserted in a path between the first circuits, wherein a threshold value of each of transistors constituting the second circuit is set so that a signal delay time between the first circuits does not exceed a given target value.